# NIELIT Virtual Academy

## *INTERSHIP PROSPECTUS*

**Name of the Internship:** Online Internship in RTL Design uisng Verilog HDL

**Internship Code**: IN13

**Mode of Conduction**: Online

**Starting Date**: 20th May 2026

**Last date of registration**: 17th May 2026

**Duration**: 6 Weeks

## Objective of the Course

✓ The internship program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL.

## Outcome of the Course

- ✓ Understand the brief history, present and future, and Design Cycle of VLSI technology.
- ✓ Learn and implement the HDL IPs using Verilog HDL from scratch.
- ✓ Emulate, debug & Characterize reusable IPs
- ✓ Provide hands-on for highly deterministic real-time applications

## Course Fee: **Rs: 1000/-(inclusive of GST)**

## Eligibility: **Pursuing an Undergraduate level course or above**

## Methodology

- ✓ Teaching Mode: Self-Pace
- ✓ Access from anywhere anytime
- ✓ Content Access through e-learning portal
- ✓ Doubt Removal Session
- ✓ Covers both Theory & Practical
- ✓ Certification: On completion of the Mini Project

## Registration Link: http://nva.nielit.gov.in

## Contact Details:

- ✓ Course coordinator Name: Mr Naresh Raja
- ✓ Email: trng.chennai@nielit.gov.in; contact.nva@nielit.gov.in
- ✓ Mobile number: **7598730125**

## Course Structure:

| Module No | Module Title |
|---|---|
| *1* | VLSI Fundamentals |
| *2* | RTL Design Methodology |
| *3* | RTL Design Using HDL |
| *4* | RTL Simulation and Verification |
| *5* | Timing Constraints and Analysis |
| *6* | Project |

## Syllabus:

### Detailed Syllabus

**Module 1: VLSI fundementals**

- Overview of VLSI technology and its significance
- Introduction to VLSI design flow: Front-end and Back-end
- Fundamentals of MOSFET operation
- CMOS Inverter Characteristics
- CMOS Logic Design
- Transistor Level Schematics and Layouts
- On-Chip Wire Modeling
- Bonding Diagram, Packaging, and Assembly
- Combinational Logic Circuit Critical Path Optimization

**Module 2: RTL Design Methodology**

- Basics of Register Transfer Level (RTL) design
- Overview of RTL design process and methodology
- Introduction to Hardware Description Languages (HDLs) – Verilog

**Module 3: RTL Design Using HDL**

- Introduction to Verilog syntax and construct
- Designing combinational and sequential logic using HDL
- Writing RTL code for basic digital circuits

**Module 4: RTL Simulation and Verification**

- Functional verification techniques for RTL designs
- Introduction to test benches and test bench development
- Simulation and debugging of RTL designs

**Module 5: Timing Constraints and Analysis**

- Introduction to timing constraints in RTL design
- Timing analysis and optimization techniques
- Setup and hold time violations and resolution

**Module 6: Project**

- Capstone project
- Project Report Submission