

NIELIT Virtual Academy

INTERNSHIP PROSPECTUS

Name of the Internship: Online Internship in HLS Programming (C/C++ based HDL Design)

Internship Code: IN14

Mode of Conduction: Online

Starting Date: 20th May 2026

Last date of registration: 17th May 2026

Duration: 6 Weeks

Objective of the Course

- ✓ Provide theoretical concepts of High-Level Synthesis (HLS)
- ✓ Provide a comprehensive understanding of HLS design flow for FPGAs
- ✓ In-system Hardware-debugging of the post-implemented design
- ✓ Case studies and projects using HLS Programming

Outcome of the Course

After successful completion of the module, the students shall be able

- ✓ Create their own IP and SoC design for FPGA implementation
- ✓ Develop their own software application with Zynq APSoC

Course Fee: Rs: 1000/- (inclusive of GST)

Eligibility: Pursuing an Undergraduate level course or above

Methodology

- ✓ Teaching Mode: Self-Pace
- ✓ Access from anywhere anytime
- ✓ Content Access through e-learning portal
- ✓ Doubt Removal Session
- ✓ Covers both Theory & Practical
- ✓ Certification: On completion of the Mini Project

Registration Link: <http://nva.nielit.gov.in>

Contact Details:

- ✓ Course coordinator Name: Mr Naresh Raja
- ✓ Email: trng.chennai@nielit.gov.in; contact.nva@nielit.gov.in
- ✓ Mobile number: **7598730125**

Course Structure:

Module No	Module Title
1	VLSI Fundamentals
2	Introduction to HLS programming
3	Combination Circuits and Test Benches using C/C++
4	Sequential Circuits Design using HLS
6	Project

Syllabus:

Detailed Syllabus

Module 1: VLSI fundamentals

- Overview of VLSI technology and its significance
- Introduction to VLSI design flow: Front-end and Back-end
- Fundamentals of MOSFET operation
- CMOS Inverter Characteristics
- CMOS Logic Design
- Transistor Level Schematics and Layouts
- On-Chip Wire Modeling
- Bonding Diagram, Packaging, and Assembly
- Combinational Logic Circuit Critical Path Optimization

Module 2: Introduction to HLS programming

- HLS Design Overview
- HLS Design Flow
- HLS ports
- Propagation delay computation using HLS
- Functions and Data Flow
- HLS Test Bench Coding,

Module 3: Combination Circuits and Test Benches using C/C++

- Basics Data Types and conditional Statements,
- Bit Precision Libraries
- Combinational loop unrolling
- Overloading and Resource Constraints

Module 4: Sequential Circuits Design using HLS

- Single Cycle Design: IP Centric Design Flow
- State Machine Implementation
- Timer, Counter, Debouncer
- Integrated Logic Analyzer
- Functional Pipelining
- Interface Synthesis,

Module 5: Project

- Capstone project
- Project Report Submission