Course code **IN15** Mode of conduction – Offline

Internship on HLS Programming

Mode of conduction	Starting date	Duration	Total fee
Offline	12 Oct 2026 12th October 2026	30 Hours 6 weeks	Rs. 8,100/- Registration cum tuition fee

Last date of registration
7th October 2026

Registration link
http://nva.nielit.gov.in

Objective of the course

To develop the skillset required for the students/professionals to work in Field-programmable gate arrays (FPGAs) and provides an opportunity to co-design applications with hardware accelerators. The main objective of this course is to design an accelerator using HLS and to optimize and speed up specific computational workloads in an efficient and flexible manner.

Outcome of the course

- Provide theoretical concepts of High-Level Synthesis (HLS)
- Custom IP and SoC design for FPGA
- Provide hands-on to solve case studies and projects in SoC Design
- Provide a comprehensive understanding of HLS design flow for FPGAs
- In-system Hardware-debugging of the post-implemented design

Course structure

30 hours across 5 modules

Module No	Module Title	Duration (Hours)
1	Image Processing	5
2	Combinational Circuits and Test Benches using C/C++	7
3	Sequential Circuit Design using HLS	7
4	Function Acceleration on FPGA	5
5	Project Work	6
	Total Duration	**30**

01 Image Processing — 5 hours

- Introduction to Image Processing, Notion of pixel, resolution, quantization, photon noise, Geometric transformations, source-to-target and target-to-source mapping, planar and rotational homography, Image registration and change detection, Motion Blur and Image Formation. Image Transform, Image Enhancement, Restoration, and Edge Detection Design Verification using Test benches. Typical image processing application implementation using MATLAB/Python

02 Combination Circuits and Test Benches using C/C++ — 7 hours

- HLS Design Overview, HLS Design Flow, HLS ports, Propagation delay computation using HLS, Functions and Data Flow, HLS Test Bench Coding, Data Types and conditional Statements, Bit Precision Libraries, Combinational loop unrolling, Overloading and Resource Constraints

03 Sequential Circuits Design using HLS — 7 hours

- Single Cycle Design: IP Centric Design Flow (Parallel to Serial and Serial to Parallel), State Machine Implementation, Sequential Circuits Design using HLS
- Timer, Counter, Debouncer, Clock Generator, Single Cycle Regular Pulses, Edge Detector, Integrated Logic Analyzer, Functional Pipelining, Interface Synthesis

04 Function Acceleration on FPGA — 5 hours

- Pipelining, Retiming, Unfolding, Folding, Scheduling, Type of scheduling, optimization and its applications.
- Loop latency, Array Partitioning, Loop Merge, Loop Pipeline

Learning outcomes

After successful completion of the module, the students shall be able

- Implement the Image Processing application using MATLAB/Python
- Use HLS concepts for designing combinational logic circuits
- Design sequential logic circuits with C/C++ language using the HLS approach
- Use C/C++ for accelerating compute-intensive algorithms on Zynq platforms

Eligibility

5th semester B.E./B.Tech (onwards) in Electronics / Electronics & Communication / Electrical / Electrical and Electronics / Instrumentation / Electronics & Instrumentation / Instrumentation & Control / Biomedical / Computer Science / Information Technology,
or **M.Sc. (Electronics)** in Electronics / Electronics, or equivalent.

Course fee

Fee Type	Fee Detail - Others	Last Date
Registration Fee cum Tuition Fee	Rs. 8,100/-	07-10-2026
Total Fee	**Rs. 8,100/-**	

Reading list

01 Parallel Programming for FPGA, The HLS Book, Ryan Kastner

02 K. K. Parhi, VLSI Digital Signal Processing, Wiley 1999

03 DSP Integrated Circuits, L. Wanhammar

04 Image Processing Methods — How To Develop Image Processing Systems Using Xilinx FPGA: Using A Zynq, Herman Sheroan, 2021

05 Exploring Xilinx FPGA And Heterogeneous SoC — The Principles Behind Image-Processing Sensors: Introduction To Image Processing, Synthia Collums, 2021

06 Pedroni, Volnei A., Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press
ISBN-10: 0262014335 | ISBN-13: 978-0262014335

Register online

http://nva.nielit.gov.in

Registration closes
7th October 2026

Course begins
12th October 2026

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Contact details

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