NIELIT Virtual Academy

INTERNSHIP PROSPECTUS

Name of the Internship: ***Internship in FPGA Prototyping using Verilog HDL and HLS [for VIT Chennai students only]***
Mode of Conduction: *offline at NIELIT Chennai*
Starting Date: *3rd June 2026*
Last date of registration: *2nd June 2026*
Duration: *4 weeks*

Objective of the Course

This internship aims to equip participants with industry-relevant skills in FPGA prototyping using Verilog HDL and High-Level Synthesis (HLS). It focuses on practical RTL design, hardware optimization, and integration of real-time digital systems through hands-on labs and mini-projects. The program prepares participants to design, simulate, and deploy FPGA-based solutions aligned with current VLSI and embedded industry practices.

Outcome of the Course:

❖ Upon completing this internship, participants will be able to design, simulate, and optimize digital systems using Verilog HDL and High-Level Synthesis on FPGA platforms.

❖They will gain hands-on proficiency in RTL design and hardware implementation, preparing them for industry roles in VLSI and embedded systems development.

Course Fee: Rs: 3000/-(inclusive of GST)

Eligibility: Pursuing BE/B.Tech at VIT Chennai

Methodology:

- ✓ Teaching Mode: offline
- ✓ Covers both Theory & Practical
- ✓ Certification: On completion of the Mini Project

Registration Link: https://nva.nielit.gov.in

* Registration via the link above is mandatory for all internship participants.

Contact Details:

- Course Coordinator Name: Ishant K Bajpai, Scientist 'D', M.Tech (VLSI)
- Email: trng.chennai@nielit.gov.in
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Course Structure:

Module No	Module Title	Duration (Week)
1	Module 1: Verilog-HDL Programming for FPGAs	2 Weeks
2	Module 2: FPGA Prototyping using HLS Programming	2 Week
Total Duration		**4 Weeks**

Syllabus:

Module 1 – Verilog-HDL Programming for FPGAs

- Review of Digital Systems: Critical Path, Setup Time, Hold Time, and Optimization Techniques
- Installation of VIVADO Software
- Introduction to Hardware Description Languages (HDLs) - Verilog; Lexical Conventions & Data Types
- System Tasks & Compiler Directives; Modules, Ports & Module Instantiation Methods
- Hierarchical Modeling Concepts; Basics of Register Transfer Level (RTL) design; Overview of RTL design process and methodology
- Designing Combinational & Sequential Logic using HDL
- Introduction to test benches and test bench development
- FIR & IIR Filter Implementation in Resourced Share Environment & KPN
- Systolic Array Architecture
- Number System Architecture - Dynamic Range, Single Precision and Double Precision Representation using various industry standards (IEEE 754, TensorFloat32 etc.)
- Case Studies: Design of a 32-bit processor
- Mini Project

Module 2 – FPGA Prototyping using HLS Programming

- Introduction to HLS Programming; HLS Design Flow
- Introduction to FPGA; Understanding the internal architecture of FPGA; Basic components of an FPGA: LUTs, flip-flops, interconnects

- C/C++ Testbench; Bit Precision Declaration; Integer Arithmetic
- Interface Synthesis; State Machines
- Denouncer & ILA in HLS
- Retiming and Pipelining
- Unfolding, Folding, and Scheduling
- Compiler Optimization
- Arrays & AXI Interface
- Mini Project

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