# NIELIT Virtual Academy

**COURSE PROSPECTUS**

**Name of the Internship:** *Introduction to Verilog Programming*
**Course Code:** SP12
***Mode of Conduction:*** *Online[Self-Paced]*
**Duration:** *24 Hours*

## Objective of the Course

This skill oriented course provides participants with the information and knowledge experience necessary to evolve as a professional. This course covers the fundamentals of Register Transfer Level (RTL) design using Verilog Hardware Description Language (HDL). It provides a practical approach as well as in-depth knowledge on RTL coding of combinational and sequential digital circuits, functional verification using test benches, and timing analysis for FPGA/ASIC based Embedded and SoC design.

## Outcome of the Course:

Provide the participants with in-depth knowledge and skills required for RTL design, functional verification and timing analysis using Verilog HDL as per Industry Standards.

## Course Fee: Rs: 600/-(inclusive of GST)

## Eligibility: 12th standard or equivalent

## Methodology:

- ✓ Teaching Mode: Instructor-Led (Live Sessions)
- ✓ Structured Day-wise Schedule with Multiple Sessions per Day
- ✓ Dedicated Hands-on Lab Sessions using Vivado Software
- ✓ Doubt Removal & Tutorial Sessions
- ✓ Covers both Theory & Practical (RTL Design, Verification and Timing Analysis)

## Registration Link: https://nva.nielit.gov.in

## Contact Details:


- Course Coordinator Name: Ms. Steny Jose
- Mobile number: 7598730125
- Email: trng.chennai@nielit.gov.in

## Contents:

**Module 1: RTL Design Fundamentals & Verilog Basics**

- Overview of RTL design process and methodology
- Installation of Vivado software
- Hierarchical modeling concepts
- Basics of Register Transfer Level (RTL) design
- Introduction to Hardware Description Languages (HDLs) - Verilog:
  - Lexical conventions & data types
  - System tasks & compiler directives
- Modules, ports & module instantiation methods

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**Module 2: Combinational & Sequential Logic Design**

- Designing combinational logic using HDL
- Designing sequential logic using HDL
- Writing RTL code for basic digital circuits
- Hands-on lab sessions on digital circuit design

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**Module 3: Behavioral Verification using Testbench**

- Behavioral verification techniques for RTL designs
- Introduction to test benches
- Test bench development:
  - Stimulus generation
  - Response checking
- Simulation and debugging of RTL designs
- Hands-on lab sessions

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**Module 4: Timing Analysis & Optimization**

- Introduction to timing constraints in RTL design
- Timing analysis and optimization techniques
- Setup and hold time violations:
  - Identification of violations
  - Resolution techniques
- Tutorial sessions as per requirement

## Examination & Certification

| Category | Theory | Project | | Total |
|---|---|---|---|---|
| Paper Name | No. of Papers:01 | Project | Presentation | |
| Marks | 40 | 30 | 30 | 100 |

**After successful completion of the course, candidate will get an online certificate with the following Grading Scheme:**

| Marks Range | Grade | Certificate Type |
|---|---|---|
| 85% and above | S | Graded |
| 75-84% | A | Graded |
| 65-74% | B | Graded |
| 55-64% | C | Graded |
| 50-54% | D | Graded |
| <50% | F | Participation |
| Attended the Course but not appeared in Examination | N | Participation |