NIELIT Virtual Academy

COURSE PROSPECTUS

Name of the Internship: *Introduction to FPGA Prototyping using Verilog HDL*
Course Code: SP13
Mode of Conduction: *Online[Self-Paced]*
Duration: *30 Hours*

Objective of the Course

The course aims to introduce participants to the fundamentals of FPGA architecture, digital design, and Verilog HDL. Participants will learn to design, simulate, synthesize, and implement digital circuits on FPGA platforms using industry-standard tools. The course emphasizes hands-on FPGA prototyping, including RTL design, timing concepts, and hardware verification. By the end of the course, participants will be able to develop and implement basic FPGA-based digital systems using Verilog HDL.

Outcome of the Course:

Participants will gain the ability to analyze and optimize RTL designs for efficient hardware implementation. They will develop practical skills in debugging, resource utilization, timing considerations, and hardware testing on FPGA platforms.

Course Fee: Rs: 600/-(inclusive of GST)

Eligibility: Pursing 3rd year B.E/B.Tech or IIIrd year B.Sc (in Electronics)

Methodology:

- ✓ Teaching Mode: Instructor-Led (Live Sessions)
- ✓ Structured Day-wise Schedule with Multiple Sessions per Day
- ✓ Dedicated Hands-on Lab Sessions using Vivado Software
- ✓ Doubt Removal & Tutorial Sessions
- ✓ Covers both Theory & Practical

Registration Link: https://nva.nielit.gov.in

Contact Details:

- Course Coordinator Name: Ms. Steny Jose
- Mobile number: 7598730125
- Email: trng.chennai@nielit.gov.in

Contents:

Module 1: Introduction to FPGAs

- Overview of Field-Programmable Gate Arrays (FPGA) and their applications
- Advantages of using FPGAs in digital design

Module 2: FPGA Architecture and Components

- Understanding the internal architecture of FPGA
- Basic components of an FPGA: Look-Up Tables (LUTs), flip-flops, interconnects etc.,
- Introduction to FPGA families and resources

Module 3: FPGA Design Flow

- Overview of the FPGA design flow and methodology
- Design entry, synthesis, placement, routing and bitstream generation
- Introduction to design constraints

Module 4: FPGA Design Optimization Techniques

- Timing constraints and analysis in FPGA designs
- Pipelining, retiming and other optimization techniques
- Trade-offs between area, power and performance

Examination & Certification

Category	Theory	Project		Total
Paper Name	No. of Papers:01	Project	Presentation	
Marks	40	30	30	100

After successful completion of the course, candidate will get an online certificate with the following Grading Scheme:

Marks Range	Grade	Certificate Type
85% and above	S	Graded
75-84%	A	Graded
65-74%	B	Graded
55-64%	C	Graded
50-54%	D	Graded
<50%	F	Participation
Attended the Course but not appeared in Examination	N	Participation