

NIELIT Virtual Academy

Course Prospectus

Introduction to Static Timing Analysis STA Fundamentals - Timing Paths - Constraints - Timing Analysis - Timing Closure			Mode of conduction Online (Self-Placed)
Course Code SP14	Starting Date 7 September 2027	Duration 7 hours	Total Fee Rs. 600/-

Objective of the Course

This skill-oriented course provides participants with the knowledge and practical experience necessary to develop a strong foundation in Static Timing Analysis (STA) for digital design. The course covers the fundamentals of timing analysis, timing constraints, clock definitions, setup and hold time analysis, timing paths, slack calculation, and timing violations. It provides a practical approach to understanding STA concepts and their application in FPGA/ASIC-based designs, with hands-on exposure to timing reports, constraint development, and timing closure techniques essential for Embedded and SoC design.

Outcome of the course

Provide participants with the knowledge and practical skills required for Static Timing Analysis (STA), including timing constraints, setup and hold analysis, timing paths, slack calculation, timing reports, and timing closure techniques as per Industry Standards.

Methodology

■ Instructor-Led Recorded Sessions

■ Structured Day-wise Learning

■ Structured Day-wise Learning

■ Doubt & Tutorial Sessions

■ Doubt & Tutorial Sessions

Eligibility

■ Currently pursuing 3rd year of undergraduate studies.

■ Completed 3rd year B.Sc. in Electronics.

Contact Details

Course Coordinator

Naresh Raja T

Email

naresh@nielitchennai.edu.in

Mobile (on Whatsapp)

9372475989

Course Structure

Module 1	Module 2	Module 3	Module 4
Introduction to Static Timing Analysis and its Application	Deviation and Analysis of Setup and Hold Timing Equation	Timing Analysis, Violation Handling, and Tcl Scripting in Vivado	Fundamentals of Tcl Scripting and Timing Constraints in Vivado

01

Introduction to Static Timing Analysis and its Application

Introduction to Static Timing Analysis (STA), timing analysis methods and applications, STA for different circuit types, timing parameters and clock characteristics.

02

Deviation and Analysis of Setup and Hold Timing Equation

Setup Timing Analysis – Ideal Clock, Destination Clock Delay & Source Clock Delay, Slack Calculation and Equation Variations; Hold Timing Analysis – Ideal Clock, Destination Clock Delay & Source Clock Delay, Slack Calculation and Equation Variations.

03

Timing Analysis, Violation Handling, and Tcl Scripting in Vivado

Timing Analysis & Project Setup in Vivado, Timing Violation Handling, Introduction to Tcl in Vivado, Essential Tcl Commands for Vivado Scripting.

04

Fundamentals of Tcl Scripting and Timing Constraints in Vivado

Tcl Strings, Lists & Arrays, Timing Constraints, Tcl Commands for Design Access, Clock Definition for Timing Analysis.

Examination & Certification

.no	Category	Marks
1	Theory	40
2	Project (Submission + Presentation)	60
Total		100

Note:

After successful completion of the course, candidate will get an online certificate with the following Grading Scheme

Marks Range	Grade	Certificate Type
> 85 %	S	Graded
75 - 84 %	A	Graded
65 - 74 %	B	Graded
55- 64 %	C	Graded
50 - 54 %	D	Graded
< 50 %	F	Participation
ABSENT	N	Participation