राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, चेन्नई
National Institute of Electronics and Information Technology, Chennai
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

Course Prospectus

Embedded & SoC Designer

VL201

NSQF LEVEL 5.5

600 Hours | 6 Month | Online Mode

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Key Details

Course Name : Embedded and SoC Designer

Course Code: VL201

Duration : 600 Hours

Last Date of Registration
1st October 2026

Date of First Selection
5th October 2026

Payment of First Instalment
on or before 6th October 2026

Course Start Date
7th October 2026

Payment of Second Instalment
on or before 15th January 2027

Registration Fee	Course Fee
General : ₹1000	General : ₹36,000
SC / ST : NIL	SC / ST : NIL

Program Overview

Government initiatives such as Make in India and India Semiconductor Mission are accelerating the growth of the semiconductor ecosystem in India. The rapid advancement of the semiconductor and electronics industries has significantly increased the demand for skilled professionals in VLSI and Embedded Systems design. With continuous developments in semiconductor process technologies, a large number of transistors can now be integrated onto a single chip, enabling the realization of highly complex Integrated Circuits (ICs) and advanced System-on-Chip (SoC) architectures.

SoCs have become the backbone of modern electronic systems and are widely used across diverse applications ranging from embedded devices to high-performance computing platforms. Emerging technologies such as artificial intelligence, machine learning, image processing, andadvanced communication systems have further increased the complexity of system design, requiring efficient integration of hardware and software components. Addressing these challenges demands engineers with strong interdisciplinary knowledge and practical design expertise. In this context, theprogram aims to provide advanced training in embedded processor architecture, hardware-software co-design, and implementation on FPGA platforms, enabling participants to develop the skills required for designing next-generation embedded and VLSI systems.

Objective of the course

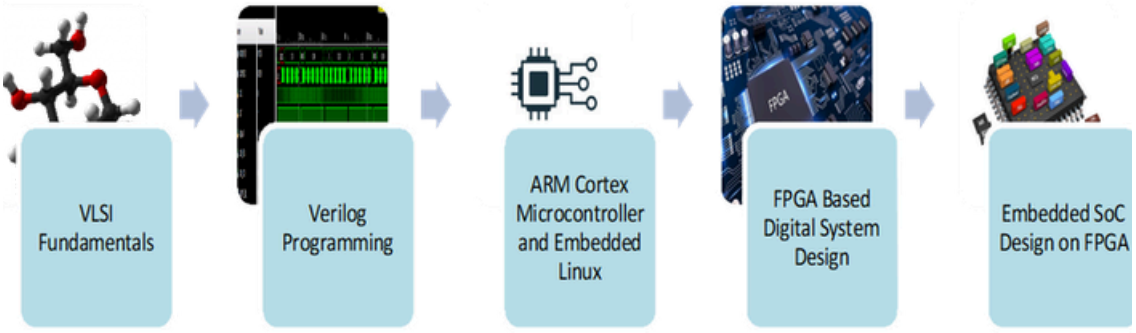
The objective of this course is to equip participants with the knowledge and practical skills required to design and implement modern embedded and System-on-Chip (SoC) based systems. The course focuses on developing competence in embedded architecture, FPGA-based design, hardware–software integration, and real-time system development using contemporary development tools and platforms. It aims to familiarize learners with current design methodologies, prototyping techniques, and validation practices used in the embedded and semiconductor industry, thereby preparing them to design and deploy efficient embedded solutions on FPGA-based target platforms.

Outcome of the course

After successful completion of this course, students will be able to:

- Develop embedded applications on ARM Cortex microcontrollers using Embedded C programming.
- Implement and analyze image processing algorithms using MATLAB.
- Design and develop VLSI IP cores using Verilog HDL and implement them on FPGA platforms.
- Create and integrate custom IP cores to build complete SoC designs for FPGA-based implementation.
- Develop and deploy software applications on Zynq APSoC platforms.

Course Progression



Course Structure

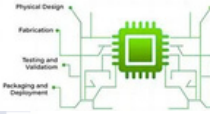
This course contains totally Eight modules. After completing the first Eight modules, the students must do a six week project using any of the topics studied to earn the PG Program in Embedded and SoC Design Certificate

MODULE 1

Code : VL201-1

Name : VLSI design Methodologies and principles

Duration : 60 Hours

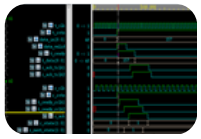


MODULE 2

Code : VL201-2

Name : Verilog Hardware Description Language (HDLs) to design RTL Circuits

Duration : 60 Hours



MODULE 3

Code : VL201-3

Name : Embedded System Design with Embedded C Programming on ARM Cortex Microcontrollers

Duration : 60 Hours

MODULE 4

Code : VL201-4

Name : Implementation of Complex Embedded Systems using Suitable Operating Systems

Duration : 60 Hours

MODULE 5

Code : VL201-5

Name : Prototype digital circuits on FPGA using HDLs, analyse and debug

Duration : 60 Hours

MODULE 6

Code : VL201-6

Name : Embedded SoC Design on FPGA

Duration : 60 Hours

MODULE 7

Code : VL201-7

Name : Employability Skills

Duration : 60 Hours

MODULE 8

Code : VL201-8

Name : Project Work/OJT

Duration : 180 Hours

Total Duration : 600 Hours

Course Fees

The course fee is **₹36,000/-** (Can be paid as a single instalment of ₹36,000/- or in 2 instalments as given below)

REGISTRAION FEE : ₹1000/- for General

REGISTRAION FEE : NIL for SC/ST Candidates

Last Date for 2st Instalment
On or before 15th January 2027

Last Date for 1st Instalment : 6th October 2026

Instalment I : ₹17,500/- for General Candidates (NIL for SC/ST Candidates)

Instalment II : ₹17,500/- for General Candidates (NIL for SC/ST Candidates)

Registration Fee

Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible

However, the above registration fee shall be refunded on few special cases as given below

- Candidates are eligible but not selected for admission
- Course postponed and new date is not convenient for the student
- Course Cancelled

Eligibility

✓ Pursuing 3rd Year of UG in Computer Science / IT / Electronics and Communication Engineering / Electrical Engineering / allied branches.

✓ Completed 3rd Year of UG in Computer Science / IT / Electronics and Communication Engineering / Electrical Engineering / allied branches.

Or

✓ Previous relevant Qualifications of NSQF Level 5 with 1.5 years' experience in relevant field

Number of Seats : 500

Note : *Seats are allocated based on the merit of the Qualification*

How to Apply?

Candidates can apply online in our website http://nva.nielit.gov.in/ Payment towards non-refundable registration fee can be paid through any of the following modes :

✓ Online transaction

ACCOUNT NAME :	*NIELIT CHENNAI*
ACCOUNT NUMBER :	*31185720641*
BANK NAME :	*State Bank of India (SBI)*
BRANCH :	*Kottur (Chennai)*
IFSC CODE :	*SBIN0001669*

✓ Pay through UPI Mobile Apps.

Note : *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

Last date of Registration : 1st October 2026

Registration Procedure

All interested candidates are required to fill the Registration form online with registration fees before ***1st October 2026*** with all the necessary information

Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The Provisionally Selected Candidates will be informed regarding *selection via email.* In case of vacancy, additional selection lists will be prepared and will be intimated by email only.
- ✓ Provisionally selected candidate must upload their document on registration portal for online verification.
  - ***Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheet.***
  - ***One passport size photograph.***
  - ***Self-attested copy of Govt. issued photo ID card***
- ✓ After document verification, selected candidates must pay first instalment of ₹.17,500/- or as applicable ***on or before 6th October 2026*** by payment mode mentioned above. Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

Admission

All provisionally selected candidates whose documents are verified and paid the fees (full or first instalment) and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credentials and URL for online portal will be shared through WhatsApp or email.

Note : *All Provisionally Selected Candidates have to visit NIELIT Chennai for Certificate Verification. Otherwise their candidature will be cancelled without any intimation.*

Discontinuing the course

- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

Course Timings

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

Address

National institute of Electronics and Information Technology
ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025
E-mail: ishant[at]nielit[dot]gov[dot]in/ Phone: 044-24421445
Contact Person: Mr. Ishant Kumar Bajpai Mobile: 9445240125 (Call @ 9 AM to 6 PM)

Course enquiries

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

Placement

Students who have completed the course successfully and qualified, will be given placement guidance and career counselling to crack the interviews.

Important Dates

Last Date of Registration	***01-10-2026***
Payment of First Instalment	***On or before 06-10-2026***
Course Start Date	***07-10-2026***
Payment of Second Instalment	***On or before 15-01-2027***

Examination & Certification

✓ Final Certificates will be issued after successful completion of all the modules including mini project. For getting certificate a candidate has to pass each module individually with minimum required marks of 50%.

Examination Scheme

Examination scheme for each module is as follows :

Module Name	Total Marks	Written	Practical / Assignment
VLSI design methodologies and principles	48	33	15
Verilog hardware description languages (HDLs) to design RTL circuits	49	34	15
Embedded System Design with Embedded C Programming on ARM Cortex Microcontrollers	49	34	15
Implementation of Complex Embedded Systems using Suitable Operating Systems	48	33	15
Prototype digital circuits on FPGA using HDLs, analyse and debug	48	33	15
Embedded SoC Design on FPGA	48	33	15
Total	290	200	90
Employability Skills	30	30	0

Grading Scheme

✓ Following Grading Scheme (based on total marks) will be followed:

Grade	S	A	B	C	D	Fail
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

✓ Final Grading as per above grading scheme will be given based on total marks obtained in all modules. For last module (VL201-8) grade will be given based on project demonstration.

Lab Infrastructure Details

Hardware Facilities

- ✓ Development Boards - STM32, ARM Cortex-M4
- ✓ Sensors–PIR, Ultrasonic, Soil Moisture, Accelerometer & Gyro meter
- ✓ FPGA- Xilinx Kintex-KC705 Evaluation Kit, Xilinx Virtex - VC 707 Evaluation Kit, ZedBoard-Zyng-7000 Development Board
- ✓ DSP Evaluation Board – TI-EVK2H with Arm Cortex-A15 processor

Software Facilities

- ✓ OpenSTM, CubeMX
- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ MATLAB
- ✓ SPICE
- ✓ Cadence Virtuoso

Student Testimonials

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JOB PLACEMENT

Dr. Sachin Bahade

Course Completed: June 2023

Assistant Professor and Head Department of Electronics,
Nabira Mahavidyalaya, Katol, Dist. Nagpur

Message

Overall the training was very excellent and I am very much thankful to NIELIT Chennai, faculties for their invaluable support and guidance throughout the coursework. It was a wonderful experience throughout the course. It was a very much interactive session by giving real-time experiences to understand it in a more practical manner. Their mentorship helped me to enhance my overall academic and professional development. I am fortunate to have had someone as acknowledgeable and supportive as them by my side during this process. The knowledge, skills, and practical experience I gained during the coursework were instrumental in preparing me for the challenges of the academic and professional world. The PG in embedded and SoC course provides thorough knowledge of embedded systems, Python, Matlab, Verilog, and VLSI design. Their dedication and commitment made a significant difference in helping me secure a position that aligned with my career goals.

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JOB PLACEMENT

NAVEEK KUMAR THARASI

Course Completed: June 2023

Senior Software Engineer, Wipro

Message

"I had the opportunity to attend PGP embedded & VLSI course at NIELIT Chennai, and I must say it was an exceptional learning experience. The course provided a comprehensive and in-depth understanding of embedded systems and VLSI design, equipping me with valuable knowledge and skills.

One of the aspects that made this course truly outstanding was the expertise and dedication of the faculty members. They were not just knowledgeable instructors but also excellent mentors. They provided guidance and support, addressing our queries and ensuring that we were able to apply the concepts practically. Their commitment to our learning journey was evident in their personalized attention and willingness to assist beyond the classroom.

I highly recommend the embedded & VLSI course at NIELIT Chennai to anyone looking to delve into these fascinating domains.

Placement Details

M Naveen Kumar Tharshi
Wipro, Bangalore
Software Engineer [VLSI]

Shivani
Velankani, Bangalore
FPGA Design Engineer

Dilip
ICSR, IIT M
Research Scientist [FPGA]

Bala Krishna
BEL, Bangalore
Project Engineer [FPGA]

Sagar Parmar
Nalanda R&D Lab
Embedded Developer

Suresh
NIOT, Chennai
Project Scientist

Sona Ragu
Continental Automotive Components
Embedded Software Engineer

Tilokesh Malik
Cybermotion Technologies, Hyderabad
Embedded Engineer

Faculty Profile

Ishant Kumar Bajpai

Scientist 'D'

Ishant Kumar Bajpai, extensive experience spans over a decade and revolves around implementing funded projects in two key areas: the Internet of Things (IoT) and Very Large Scale Integration (VLSI) with applications in the Biomedical and Automotive industries. His research interests are focused on FPGA implementations of Digital Signal Processing (DSP) systems.

Steny Jose M

Project Engineer - VLSI

Steny Jose M, holds M.E in Power Electronics and Drives and has completed a Postgraduate Programme from Indian Institute of Bangalore. She has 1 year of experience as an Assistant Professor and over 4 years of experience as a Subject Matter Expert. Her expertise includes Digital and Analog circuit design, FPGA prototyping, and working with industry tools such as Xilinx Vivado and Cadence Design System tools. She has also worked on the design of Neuromorphic computing ASIC for specialized applications.

Raghavendran S

Project Engineer - RPA

Raghavendran S, with 7 years of experience bridging the gap between hardware and software automation. Expertise spans across Robotic Process Automation (RPA), Embedded Systems, and the Internet of Things (IoT). Leveraging a foundational background in Electronics and Instrumentation, he specializes in designing and delivering high-impact training sessions and hands-on laboratory modules.

Prasanth B R

Project Engineer - IoT

Prasanth B, with 8 years of experience in Embedded Systems and IoT. He holds Masters in Embedded Systems and a Bachelor's in CSE, with expertise in Embedded C, ARM Cortex, Embedded Linux, and RTOS. Prior to NIELIT, he served as a Research Fellow at DRDO and his professional interests span IoT applications, VLSI, ARM Cortex programming, and IoT data analysis, with a strong focus on practical, industry-aligned solutions.

Detailed Syllabus of the Course

VL201-1 : VLSI design methodologies and principles

Duration : 60 Hours

Objective : The objective of the module is to provide a detailed review of VLSI fundamentals for a thorough understanding of the concepts and techniques for analog and - digital system design.

Module Description

Introduction to VLSI Design

- Overview of VLSI technology and its significance
- Introduction to VLSI design flow: Front-end and Back-end

CMOS Transistor Theory

- Fundamentals of MOSFET operation
- MOSFET characteristics and modeling
- MOSFET scaling trends and technology advancements

CMOS Inverter Characteristics

- CMOS inverter operation and voltage transfer characteristics
- Noise margin analysisand power consumption considerations
- Inverter sizing and optimization techniques

CMOS Logic Design

- Introduction to basic logic gates: AND, OR, NAND, NOR
- Combinational logic design using CMOS technology
- Designing complex logic functions using CMOS logic gates

Transistor Level Schematics and Layouts

- Transistor level design techniques
- Schematic design and layout considerations
- Design rules, metal layers, and interconnect routing

On-Chip Wire Modeling

- Introduction to on-chip interconnects
- Wire parasitics and their impacton circuit performance
- Modeling and simulation of on-chip wires

Bonding Diagram, Packaging, and Assembly

- Overview of packaging technologies and assembly processes
- Bonding diagram design and considerations
- Packaging trends and challenges

Gate Delays and Logical Effort

- Gate delay modeling and estimation
- Introduction to logical effort analysis
- Determining the best delay-power trade-off for logic gates using P/N ratio

Combinational Logic Circuit CriticalPath Optimization

- Identifying criticalpaths in combinational circuits
- Gate sizing and logic restructuring techniques
- Timing optimization for improved performance

Timing in Sequential Circuits

- Introduction to sequential circuits: flip-flops, registers
- Setup and hold time analysis
- Sequential circuit timing considerations and optimization techniques

Learning Outcomes

The Qualifier of the NOS shouldbe able to:

- Construct digital logic gates using CMOS technology
- Analyze and optimize the performance of digital gates
- Anticipate the impact of parasitics and technology scaling
- Implement a semi-custom integrated circuit from a given RTL code to layout
- Link simplified abstract models to detailed computer simulations

Reading List

1. Design of Analog CMOS ICs - Razavi. The best book available on CMOS analog.
2. Microelectronic circuits: Adel Sedra and Kenneth C. Smith
3. Franco S, Design with Operational Amplifiers and Analog Integrated Circutis
4. CMOS Analog circuit design - Allan and Holberg
5. Analog Integrated Circuit Design - Ken Martin and David Johns
6. Digital Design by Morris Mano & Michael D Ciletti
7. Digital Design: Principles and Practices by John F. Wakerly
8. Digital Design by Frank Vahid

VL201-2 : Verilog hardware description languages (HDLs) to design RTL circuits

Duration : 60 Hours

Objective : The objective of the course is to provide a thorough understanding of and hands-on with digital design & Verification using Verilog HDL

Module Description

RTL Design Methodology

- Basics of Register Transfer Level (RTL) design
- Overview of RTL design process and methodology
- Introduction to Hardware Description Languages (HDLs) - Verilog

RTL Design Using HDL:

- Introduction to Verilog syntax and construct
- Designing combinational and sequential logic using HDL
- Writing RTL code for basic digital circuits

RTL Simulation and Verification:

- Functional verification techniques for RTL designs
- Introduction to test benches and test bench development
- Simulation and debugging of RTL designs

Timing Constraints and Analysis:

- Introduction to timing constraints in RTL design
- Timing analysis and optimization techniques
- Setup and hold time violations and resolution

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax, Level of Abstraction in Verilog programming and test bench simulation.
- Design and Develop IPs for VLSI using Verilog
- Emulate, debug & characterize reusable IPs

Reading List

1. Verilog HDL - A guide to Digital Design and Synthesisby Samir Palnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi
5. Fundamentals Of Digital Logic With Verilog Design by Stephen Brown
6. Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL by MichaelD. Ciletti
7. The Verilog Hardware Description Language by Donald E. Thomas & PhilipR. Moorby
8. IEEE Std 1364-2005 : IEEE Standard Hardware Description Language based on the Verilog Hardware Description Language by the IEEE

VL201-3 : Embedded System Design with Embedded C Programming on ARM CortexMicrocontrollers

Duration : 60 Hours

Objective : To set the required background in embedded system concepts, Embedded 'C' language such as Memory Management, Pointers, Data structures, and architecture of the ARM Cortex processor for highly deterministic real-time applications.

Module Description

'C' and Embedded C:

Introduction to 'C' programming, Storage Classes, Data Types, Control Structures, Arrays, Functions, Memory Management, Pointers, Pointer to Functions and advanced topics on Pointers, Structures and Unions, Data Structures, Linked List, Stacks, Queues, Pre-processor directives, File operations, Variable arguments in Functions, Command line arguments, bitwise operations, Typecasting.

Embedded Concepts:

Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of Embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools.

Introduction to ARM Cortex Architecture:

Introduction to 32-bit Processors, The ARM Architecture, Overview of ARM, Overview of Cortex Architecture, Cortex M4 Register Set and Modes, Cortex M4 Processor Core, Data Path and Instruction Decoding, ARM Cortex M4 Development Environment, Assembler and Compiler, Linkers and Debuggers, ARM, Thumb & Thumb2 instructions, Mixing ARM & Thumb Instructions, Memory hierarchy, Memory Mapping, Cache.

Cortex M4 Microcontrollers & Peripherals:

Cortex M4-based controller architecture, Memory mapping, Cortex M4 Peripherals – RCC, GPIO, Timer, System timer, UARTs, LCD, ADC, Cortex M4 interrupthandling –NVIC. Application development with Cortex M4 controllers using standard peripheral libraries.

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Participants will be able to develop Embedded applications using Embedded C Programming
- Participants will be able to use ARM Cortex-Mx based Microcontrollers with Embedded C Programming for Application Development

Text Books:

1. Embedded/Real-Time Systems Concepts, Design and Programming Black Book,Prasad, KVK.
2. Let us C by YashwantKanetkar.

The Definitive Guide to the ARM Cortex M3, Joseph Yiu, Newnes

Reference Books:

1. Embedded SystemsArchitecture Programming and Design: Raj Kamal, TataMcGraw Hill.
2. Embedded C, Pont, Michael J
3. Embedded Systems an IntegratedApproach: Lyla B Das, Pearson
4. C Programming language, Kernighan, Brian W, Ritchie,Dennis M
5. Art of C Programming, JONES, ROBIN,STEWART, IAN
6. ARM System Developer's Guide - Designing and Optimizing System Softwareby: Andrew N Sloss, Dominic Symes, Chris Wright; 2004, Elseiver.
7. Cortex M3/M4 Reference manual.
8. STM32Ldiscovery datasheets, reference manuals & Application notes.

VL201-4 : Implementation of Complex Embedded Systems using suitable Operating Systems

Duration : 60 Hours

Objective : To Skill the students in Configure, Deploying, and Debugging the Linux OS onto a Target Board to build a completeEmbedded Product using Linux Kernel.

Module Description

'Introduction:

Basic Operating System Concepts, History & Benefits of Linux, Fundamentals of Embedded Linux OS, Comparison of Embedded OS, Embedded OS Tools and IDE, Embedded Linux, Applications and Products.

Architecture of Embedded Linux:

Types of kernels, Kernel Architecture Overview: User Space, Kernel Space, Kernel Functional Overview: File System, Process Management, Address Spaces and Privilege Levels, Memory Management, System Call, Inter Process Communication (IPC) – Pipes, FIFO & Shared Memory, Device Drivers, Network.

Commands in Linux:

Log in Linux system and Log in Remote Linux Systems-Getting Help Accessing & Working with the Command Line and Shell System Access, Entering Commands.

Boot Methods:

Creating User Accounts &Managing Users Creating Groups & Managing Groups, Directory Management, File Permissions and Ownership, Text Editor.

Configuringthe Linux Environment:

Linux environment, Types of Hosts, Types of Host/Target Development Setups, Types of Host/Target Debug Setups, Embedded Environment Tools, GNU Tool-chain Cross Compilers.

Tool-chain:Configuration and Cross-Compilation:

Tool-chain. Native vs. cross-compilation, Toolchain Components, Toolchain choices, Using build root to build the tool chain, Configuration options, Adding path variables to start up scripts (.bashrc), CROSS_COMPILE variable, Validating the cross-compiler.

Linux Bootloader & U-Boot:

Boot-loader Phases, U-boot – Embedded boot loader, Navigating the u-boot sources, Configuring and Cross-compiling u-boot, installing u-boot on the target, understanding u-boot commands, changing environment variables to setup kernel booting, transferring files to the target using tftp.

Embedded Linux Kernel:

Kernel Features, Kernel Subsystems, Memory Manager, Scheduler, Embedded Storage, I/O Subsystem, Network Subsystem, Navigating the kernel sources, Kernel Configuration, Kernel Compilation Booting the kernel using u-boot, Module compilation and Installation to RootFS, Procedure for adding a new driver to the kernel, Applying patches.

Building Root File System:

Introduction to File system, Linux directory structure, Organization and Important directories, /dev file system, Steps after kernel booting, init and start-up scripts, Downloading & Compiling RootFS, RootFS in Flash/SD Card Storage.

Embedded Linux Kernel:

Kernel Features, Kernel Subsystems, Memory Manager, Scheduler, Embedded Storage, I/O Subsystem, Network Subsystem, Navigating the kernel sources, Kernel Configuration, Kernel Compilation Booting the kernel using u-boot, Module compilation and Installation to RootFS, Procedure for adding a new driver to the kernel, Applying patches.

Porting OS in ARM Board:

Kernel Compilation, Booting the kernel using u-boot, Porting Linux in ARM Board.

Embedded Linux Application Programming:

Application Developments using Input Devices, Application Developments using Output Devices, Application Developments using Peripherals.

Learning Outcomes

After successful completion of this module, Students will be able to:

- Set up a Linux environment for ARM-based TargetBoards
- Configure Tool-Chain for ARM Platforms.
- Understand Linux Booting Process and be able to configure Linux Kernels on ARM-based Embedded Boards.
- Develop ARM-based Embedded Applications with Linux OS.

Reading List:

1. GNU/LINUX Application Programming, Jones, M Tims
2. Embedded Linux: Hardware, Software, and Interfacing, Hollabaugh, Craig,
3. Building Embedded Linux Systems: Yaghmour, Karim
4. Embedded Software Primer: Simon, David E.
5. Linux Kernel Internals: Beck, Michael At Al
6. UNIX Network Programming: Steven, Richard
7. Linux: The Complete Reference: Petersen, Richard
8. Linux Device Drivers: Rubini, Alessandro, Corbet, Jonathan
9. Linux Kernel Programming: Algorithms and Structures of version 2.4: Beck,Michael At Al
10. Linux Kernel Development: Love, Robert
11. Operating System Concepts, Peter B. Galvin, Abraham Silberschatz, GergGagne, Wiley Publishers

VL201-5 : Prototype digital circuits on FPGA using HDLs, analyze and debug Design

Duration : 60 Hours

Objective : The objective of the course is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation

Module Description

Introduction to FPGAs:

- Overview of Field-Programmable Gate Arrays (FPGAs)and their applications
- Advantages of using FPGAs in digital design

FPGA Architecture and Components:

- Understanding the internal architecture of FPGAs
- Basic components of an FPGA: Look-UpTables (LUTs), flip-flops, interconnects, etc.
- Introduction to FPGA families and resources

FPGA Design Flow:

- Overview of the FPGA design flow and methodology
- Design entry, synthesis, placement, routing and bitstream generation
- Introduction to design constraints

FFPGA Design Optimization Techniques:

- Timing constraints and analysis in FPGA designs
- Pipelining, retiming and other optimization techniques
- Trade-offs between area, power and performance

Learning Outcomes

After successful completion of this module, students should be able to:

- Construct digital logic circuit using Verilog HDL
- Simulate those designs using industry-standard simulation tools
- Synthesis and port the design onto FPGA using industry-standard tools
- Implementation of project of good complexity onto FPGA
- Debug the FPGA Designs with advanced FPGA tools.

Reading List:

1. FPGA-Based System Design by Wayne Wolf
2. Advanced FPGA Design Architecture, Implementation and optimization byKilts
3. Xilinx® User guides & documentation available at https://www.xilinx.com/support/documentationnavigation/overview.html
4. Intel® FPGA User guides & documentation available at https://www.intel.com/content/www/us/en/programmable/documentation/lit-index.html
5. Swadeshi Microprocessors user guides & documentation available at available at https://shakti.org.in/
6. Embedded Core Design with FPGAs. by Zainalabedin Navabi
7. FPGA Prototyping by Verilog Examples by Pong P. Chu
8. Digital Design Using Digilent FPGA Boards Verilog / Vivado Edition RichardE Haskell, Darrin M Hanna
9. FPGA Design: Best Practices for Team-Based Reuse by Philip AndrewSimpson

VL201-6 : Embedded SoC Design on FPGA

Duration : 60Hours

Objective : FPGA chips are especially useful for machine learning and Image processing. The objective of this module is to enable the qualifier to optimize throughput and adapt processors to meet the specific needs of different Image processing/ML architectures.

Module Description

Image Processing:

Introduction to Image Processing, Notion of pixel, resolution, quantization, photon noise,Geometric transformations, source-to-target and target-to-source mapping, planar and rotational homography, Image registration and change detection, Motion Blur and Image Formation. Image Transform, Image Enhancement, Restoration, and Edge Detection Design Verification using Test benches. Typical image processing application implementation using MATLAB/Python

Combination Circuits and Test Benches using C/C++:

HLS Design Overview, HLS Design Flow, HLS ports, Propagation delay computation using HLS, Functions and Data Flow, HLS Test Bench Coding, Data Types and conditional Statements, Bit Precision Libraries, Combinational loop unrolling, Overloading and Resource Constraints

Sequential Circuits Design using HLS

Single Cycle Design: IP Centric Design Flow (Parallel to Serial and Serial to Parallel), State Machine Implementation, Sequential Circuits Design using HLS Timer, Counter, Debouncer, Clock Generator, Single Cycle Regular Pulses, Edge Detector, Integrated Logic Analyzer, Functional Pipelining, Interface Synthesis

Function Acceleration on FPGA

Pipeling, Retiming, Unfolding, Folding, Scheduling, Type of scheduling, optimization and its applications. Loop latency, Array Partitioning, Loop Merge, Loop Pipeline, Nested Loop Filtering, Data/Memory Dependencies, Case Studies and Mini-Project

Learning Outcomes

After successful completion of the module, the students shall be able

- Implement the Image Processing application using MATLAB/Python
- Use HLS concepts for designing combinational logic circuits
- Design sequential logic circuits with C/C++ language using the HLS approach
- Use C/C++ for accelerating compute-intensive algorithms on Zynq platforms

Reading List:

1. Parallel Programming for FPGA, The HLS Book, Rayan Kastner
2. K. K. Parhi, VLSI Digital SignalProcessing, Wiley 1999
3. DSP Integrated Circuits, L. Wanhammar
4. Image Processing Methods - How To DevelopImage Processing SystemsUsing Xilinx FPGA: Using A Zynq, Herman Sheroan,2021
5. Exploring Xilinx FPGA And Heterogeneous SoC - The Principles Behind Image- Processing Sensors: Introduction To Image Processing, Synthia Collums, 2021
6. Pedroni, VolneiA., Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press, ISBN-10:0262014335 | ISBN-13: 978-0262014335

VL201-8 : Project Work/OJT

Duration :180 Hours

Module Description

The students can select hardware, software or system level projects. The project can be implemented using FPGAs, Microcontrollers, Open Source Hardware Platforms and Embedded Operating Systems which students have studied and used during the course.

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